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EXAMINER	
WONG, LINDA	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/678,685	DOUMA ET AL.	
	Examiner	Art Unit	
	LINDA WONG	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 2/28/2008 have been fully considered but they are not persuasive.

   a. Regarding claim 14, the applicant contends

> "The Examiner repeated the same rejection almost verbatim as it appeared in the previous Office Action. *See Office Action,* p. 9. As noted in Applicants' previous response, however, **the rejection completely fails to specify what element(s) of *Wang* purportedly correspond to the** claimed "synchronization signal." The response to arguments section of the Office Action similarly fails to clarify what, if any, **portion(s) of *Wang* are** believed by the Examiner **to correspond to the** claimed "synchronization signal."
>
> As one possibility, it might be the case that the Examiner is implying that a signal is inherently output by PLL 3 and received by phase-locked loop (PLL) detection circuit 17, which in turn produces an unlocked or locked signal. *See Office Action,* p. 3 ("The status of the phase locked loop must be determined in order to output a signal indicating an unlocked or locked signal.") However, the Examiner has not established that *Wang* teaches the particular nature of any signals that might be passed between PLL 3 and PLL detection circuit 17, much less whether any such signal is a "synchronization signal," as claimed. Moreover, the Examiner has not pointed to any teaching in *Wang* that the Examiner believes to correspond with the specific claim limitation of "determining whether [a PLL 3 output signal] is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency."
>
> Therefore, should the Examiner continue to allege that *Wang* teaches a "synchronization signal," as claimed, **clarification is respectfully requested as to where *Wang* purportedly discloses a "synchronization signal" and where *Wang* allegedly discloses determining whether the signal is "caused by the phase locked loop lockin~ onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency,"** as claimed.
>
> Since the Examiner has failed to establish that *Wang* discloses each and every element of claim 14, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(e) should be withdrawn."

The examiner respectfully disagrees. The applicant indicates clarification is needed to determine the equivalence of the "synchronization signal" recited in the claim and Wang et al. Paragraph 35 as previously indicated by the examiner discloses the following "Further logic circuitry in the form of an AND gate 20, assesses the outputs of the PLL detection circuit 17 and the line detection circuit 18 and provides a control signal to the first phase detector

control circuit 19 accordingly." Paragraph 33 discloses "The PLL detection circuit 17 determines whether the PIF PLL 3 is in a locked state. An output "1" indicates that it is in a locked state whereas a "0" indicates that it is in an unlocked state." We know the following from the two paragraphs 1) the detection circuit, label 17, indicates the status of the PLL (locked or unlocked) 2) The signal outputted from the PLL is outputted based on the output from label 17 and label 18 3) the AND gate outputs a control signal, which indicates the locked status of the PLL, to the label 19, wherein label 19 indicates to the phase control loop, label 6, to pass the h.sync signal. Based on this information we can assess the following. Fig. 2, label 17 is connected to the PLL. The synchronization signal is the output from the PLL to the detection signal. Conventionally, the output of the PLL (input to the separator 5) would be the synchronization signal, since it is well known to one skilled in the art that determining whether the PLL is locked or unlocked must be determined by using output of the PLL. To prove such a statement, the applicant is directed to look at Patent No.: 4996596. (**Note**: Patent No.: 4996596 is not being provided as part of the rejection of claim 14, but as a documentation of conventional detection circuit for determining the locked status of the PLL.) Based on the output from the PLL circuit, label 3, the detection circuit label 17 outputs a PLL_S to indicate the locked status of the PLL, label 3. A logic control signal (paragraph 35) outputted by label 20 (AND gate) outputs the locked status of label 3 is inputted into the detection control circuit label 19. Label 19 then

indicates to the phase control loop that the h.sync signal generated by PLL, label 3 can be outputted for further process.

b. Regarding claim 1, the applicant further contends

> "Amended claim 1 recites, among other things, "... a phase locked loop adapted to...keep [a] synchronization signal asserted as long as the phase locked loop is locked onto a data signal; and a timing circuit adapted to measure a period of time that the synchronization signal is asserted and to produce a lock signal if the synchronization signal is asserted for at least a specified period &time."
>
> The Examiner asserted that *Wang* discloses a circuit that produces a lock signal if a synchronization signal is asserted for at least a pause time, Tp. *See Office Action,* p. 10. However, as with claim 14 discussed above, it is unclear from the Examiner's remarks **what portion of *Wang* is believed by the Examiner to correspond to the claimed "synchronization signal." Thus, clarification on this point is respectfully requested."**

The rebuttal above describes the examiner's equivalence of the recited limitation "synchronization signal" with Wang et al's invention. Please refer to the rebuttal above.

c. Regarding claim 9, the applicant further contends

> "Claim 9 recites, among other things, *"a* controller chip having a phase locked loop that ... is adapted to operate in a locked mode that asserts the synchronization signal so long as the phase locked loop is locked onto a data signal; and a translation circuit that converts the synchronization signal from the controller chip to a lock signal ...." In contrast, the Examiner has not established that Wang discloses the aforementioned limitations. For example, the Examiner has not pointed to any description in Wang that the Examiner believes to correspond to the claimed "translation circuit."
> In the Examiner's response to arguments, various different circuits/components of Wang are discussed, including detector circuit 7, control circuit 19, and horizontal oscillator 8. However, the Examiner has not specified which of these, if any, is believed to correspond to the claimed "translation circuit," thus leaving Applicants to guess at what the Examiner believes to be the correspondence between Wang and the elements of claim 9. This much, however, Applicants respectfully decline to do, inasmuch as the burden to establish prima facie obviousness is the burden of the Examiner. Accordingly, should the Examiner continue to maintain the same ground of rejection against claim 9, Applicants respectfully request, in the interests of compact prosecution, that the Office **identify, with specificity sufficient to support a prima facie case of obviousness, which element(s) of Wang the Examiner believes to correspond to the claimed "translation circuit."**
> Applicant notes further that the Examiner has not shown that Van Roon, Lee, and IBM TDB, each relied on for their alleged teaching of various other claim limitations, cures the deficiencies of Wang. Accordingly, Applicants respectfully submit that the Examiner has failed to set forth aprima facie case for obviousness and respectfully submit that the rejection of claim 9, and corresponding dependent claims 10-13, should be withdrawn.

The examiner respectfully disagrees. The limitation recites "a translation circuit that converts the synchronization signal from the control chip to a lock signal usable by the host device, wherein a logic level of the lock signal is asserted when the phase locked loop is locked onto a data signal and is de-asserted when the controller asserts the synchronization signal in hunting mode". As per the rebuttal above, the examiner points the applicant in the direction of paragraphs 33 and 35, wherein such paragraph describes the translation circuit. Please refer to the rebuttal above for further explanation.

d. Regarding claims 15-18, the applicant contends

"Applicants respectfully submit that insofar as the rejections of claims 15-18 rely on the unsupported assertions regarding the disclosure of *Wang* advanced by the Examiner in connection with the rejection of claim 14, such rejection lacks an adequate foundation, for at least the reasons outlined at section II above. Furthermore, the Examiner has not shown that *van Roon, Lee,* and *IBM TDB,* each relied on for their alleged teaching of various other claim limitations, cures the deficiencies of *Wang.* Accordingly, the rejections of claims 15-18 should be withdrawn.

The examiner respectfully disagrees. The examiner would like to point to the rebuttal of claim 14.

e. Regarding claims 19-20, the applicant contends

"The Examiner rejected claims 19 and 20 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,794,944 to *Hirai ("Hirai")* in view of *van Roon;* rejected claim 21 as being unpatentable over *Hirai* and *van Roon,* as applied to claim 20, and further in view of *Transistors Tutorial;* and rejected claims 22-26 as being unpatentable over *Hirai* and *van Roon,* as applied to claim 19, and further in view of *IBM TDB.*

Applicants traverse the Examiner's rejections for obviousness on the grounds that a person of ordinary skill in the art would have no reason to combine the prior art elements in the manner claimed because the proposed combination would render *Hirai* unsatisfactory for its intended purpose.

Claim 19 requires, among other things, *"a* comparator circuit adapted to compare the output signal [from a timing circuit] with a reference signal such that a lock signal is not asserted unless the comparison of the output signal with the reference signal indicates that the period of time that the synchronization signal is asserted exceeds a minimum period of time."

> The Examiner proposed combining a comparison circuit 23 in *Hirai* with a timing circuit in *van Roon*. *See Office Action*, p. 18. However, comparison circuit 23 compares count values of counters 21 and 22 *(see Hirai,* Abstract), whereas the timing circuit of *van Roon* outputs a timing pulse having a predetermined duration time *(see van Roon,* p. 7). As presently understood then, the combination proposed by the Examiner would result in a configuration where the comparison circuit 23 *of Hirai* would compare a count value from one of counters 21 and 22 with the timing pulse from the *van Roon* timing circuit. However. it is not apparent that a count value *(Hirai)* is the same as a timing pulse *(van Roon),* nor has the Examiner established as much. Thus, the comparison performed by the modified circuit 23 *of Hirai* would not be feasible and/or would at best yield meaningless results and the device would be unsatisfactory for its intended purpose of optimizing a lock detection time. *See Hirai,* Abstract.
>
> Furthermore, the Examiner has not shown that *Transistors Tutorial* and *IBM TDB,* each relied on for their alleged teaching of various other claim limitations, fail to cure the deficiencies of the proposed combination of *Hirai* and *van Roon.* Accordingly, Applicants respectfully submit that the Examiner has failed to set forth a *prima facie* case of obviousness and respectfully request that the rejection of claim 19, and corresponding dependent claims 20-26, be withdrawn."

The examiner respectfully disagrees. Fig. 1 shows the counters provide a count value based on the reference signal (label reference signal) and feedback or timing signal (label feedback signal). Since the counters output values that are based on the reference and feedback signal, the comparator would be comparing the transitions from those two signals. The claimed limitation does not indicate the reference signal and the feedback cannot be altered or changed form. The recited limitation only indicates that the reference signal is compared with the output signal from the timing circuit.

2. Based on the rebuttal above, the prior art rejections stand as stated. A copy is provided below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claim 14** is rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (U.S. Pub. No. 2004/0179138).

   a. **Claim 14**, Wang discloses

   - receiving an asserted synchronization signal from a phase locked loop, the phase locked loop disposed on the controller chip (abstract, lines 5-6, 9-11, 12-15);
   - determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency (abstract, lines 5-6, 9-11, 12-15, [0053])
   - asserting a lock signal if the phase locked loop has locked onto a data signal ([0051]-[0053], the synchronization signal from the synchronization phase locked

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-3, 9, 10, and 15** rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) in view of Van Roon (NPL).

   a. **Claims 1,9**, Wang discloses:

   - a controller chip that includes a phase locked loop adapted to operate in a hunting mode and a locked mode (abstract, lines 2-4 describes search, or hunting, mode, abstract, lines 6-11 describe locked mode)
   - the phase locked loop asserts a synchronization signal in the hunting mode when a hunting frequency passes through a data signal frequency (abstract, lines 5-6, 9-11, 12-15)
   - the phase locked loop keeps the synchronization signal asserted as long as the phase locked loop is locked onto a data signal ([0053]);
   - produces a lock signal if the synchronization signal is asserted for a least a specified period of time ([0051]-[0053], the synchronization signal from the synchronization phase locked loop is asserted if the valid channel frequency is held for a predetermined time, Tp).
   - Wang fails to disclose and a timing circuit that measures a period of time, Tp, that the synchronization signal is asserted, however, Van Roon discloses a simple timer for timing a signal (p. 2, fig. 3). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

b. **Claim 2**, Wang fails to disclose a timing circuit which is an analog timer comprising a capacitor and a resistor network. However, an analeg timer which includes a capacitor and a resistor network is extremely well known in the art. Van Roon discloses a analog timer with a capacitor and resistor network (p. 2, fig. 3). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

c. **Claim 3**, although Wang fails to disclose the timing circuit comprises a transistor for resetting the timing circuit, Van Roon discloses a transistor for resetting the circuit (p. 3, 4-2, pin 4 is reset by transistor Q25). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

d. **Claim 10**, Wang further discloses the translation circuit comprising a timer that measures a period of time that the synchronization signal is asserted ([0051]-[0053], the synchronization signal from the synchronization phase locked loop is asserted if the valid channel frequency is held for a predetermined time, Tp).

e. **Claim 15**, Wang further discloses determining that the synchronization signal is caused by the phase locked loop locking onto the data signal if the period of time that the synchronization signal is asserted is greater than a specified

period of time ([0051]- [0053], the synchronization signal from the synchronization phase locked loop is asserted if the valid channel frequency is held for a predetermined time, Tp);

Wang fails to disclose measuring a period of time that the synchronization signal is asserted, Tp, however, Van Roon discloses a simple timer for timing a signal (p. 2, fig. 3). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, Stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

5. **Claims 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) and Van Roon as applied to claim 3"above, and further in view of Transistors Non-Patent Literature.

   a. **Claim 4**, Van Roon fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN transistor are well known in the art as low cost transistor with low power consumption at low voltage levels, it would have been obvious to one skilled in the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Van Roon and Wang.

b. **Claim 5**, Van Roon fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is a field effect transistor (p. 3, FET's as Transistors). Because FET transistor are well known in the art as low cost transistor which canoperate at high voltage levels, it would have been obvious to one skilled in the art at the time of invention to incorporate a FET transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Van Roon and Wang.

6. **Claims 16 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) as applied to claim 14 above, and further in view of Lee (U.S. Patent No. 5,886,748).

a. **Claim 16**, although Wang fails to disclose an input level detector that compares the synchronization signal with a reference signal and produces logical signals that may be fed into the timing circuit, Lee discloses comparing the synchronization signal with a reference signal and producing logical signals that may be fed into the timing circuit (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

b. **Claim 17**, although Wang fails to disclose comparing the lock signal with a reference signal to produce the lock signal, Lee discloses comparing the lock signal with a reference signal to produce the lock signal (col. 2, lines 51-55).

Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

7. **Claim 6, 7, 11, and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) and Van Roon (NPL) as applied to claim 2 above, and further in view of Lee (U.S. Patent No. 5,886,748).
   a. **Claims 6, 11, 12**, neither Wang nor Van Roon disclose an input level detector that compares the synchronization signal with a reference signal and produces logical signals that may be fed into the timing circuit, Lee discloses comparing the synchronization signal with a reference signal and producing logical signals that may be fed into the timing circuit (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.
   b. **Claim 7**, neither Wang nor Van Roon disclose a comparator that receives a signal from the capacitor and resistor network and a reference signal as input and that outputs the lock signal to the host device based on the value of the reference signal compared to the signal from the capacitor and resistor network, Lee discloses comparing the a timing signal such as that which comes from the capacitive resistive network as disclosed by Van Roon with a reference signal and producing logical timing signals (col. 2, lines 51-55). Because this signal

allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

8. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138), Van Roon (NPL), and Lee (U.S. Patent No. 5,886,748) as applied to claim 7 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

   a. **Claim 8**, neither Wang, nor Van Roon, nor Lee disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes alogical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). Thedisclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Wang, Van Roon and Lee.

9. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (u.s. Pub. No. 2004/0179138), Van Roon (NPL), and Lee (U.S. Patent No. 5,886,748) as applied to claim 12 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

   a. **Claim 13**, neither Wang nor Lee disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Wang and Lee.

10. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) as applied to claim 14 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

   a. **Claim 18**, Wang fails to disclose a comparator includes feedback that ch.anges a logical level of the lock signal output to the host device when the value of the

lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the invention of Wang.

11. **Claims 19,20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US Patent No.: 6794944) in view of Van Roon (NPL).

    a. **Claim 19**, Hirai discloses

    - "a comparator circuit that compares the output signal with a reference signal such that a lock signal is asserted based on the comparison of the output signal with the reference signal" (Fig. 1, label 23, Abstract discloses "a comparison circuit 23 for inputting and comparing count values of the counters 21 and 22 and outputting a control signal in an active state when the count value of the counter 21 is a first value and the count value of the counter 22 is the first value." The comparison compares the reference signal and feedback signal and determines the PLL is locked when the

count value reaches a predetermined reference count value, wherein the predetermined reference count value is based on the time length of the count period signal pulse. (Col. 1, lines 59-67))

Hirai fails to disclose

- a timing circuit that measures a period of time that a signal is asserted
- the timing circuit uses a capacitor
- wherein the timing circuit generates an output signal having a voltage across the capacitor
- comparison indicates that the period of time that the synchronization signal is asserted exceeds a minimum period of time.

However, Van Roon discloses

- a timing circuit that measures a period of time that a signal is asserted (fig. 2, 3)
- the timing circuit uses a capacitor (p. 2, fig. 3)
- wherein the timing circuit generates an output signal having a voltage across the capacitor (see pin 3 output of fig. 4-2)
- comparison indicates that the period of time that the synchronization signal is asserted exceeds a minimum period of time (Page 9 describes the lower comparator, wherein the frequency or time is adjusted based on the capacitor and resistors. Fig. 3 shows the lower comparator.)

Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it

would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Hirai.

b. **Claim 20**, although Hirai fails to disclose the timing circuit comprises a transistor for resetting the timing circuit, Van Roon discloses a transistor for resetting the circuit (p. 3, 4-2, pin 4 is reset by transistor Q25). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Hirai.

12. **Claim 21** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai in view of Van Roon (NPL) as applied to claim 20 above, and further in view of Transistors Non-Patent Literature.

a. **Claim 21**, Van Roon fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN transistor are well known in the art as low cost transistor with low power consumption at low voltage levels. It would have been obvious to one skilled in the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Van Roon and Hirai.

13. **Claims 22-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai in view of Van Roon (NPL) as applied to claim 19 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

    a. **Claims 22, 23**, neither Hirai nor Van Roon, nor Lee disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Van Roon and Hirai.

    b. **Claim 24**, Hirai discloses comparing the synchronization signal with a reference signal and producing logical signals that may be fed into the timing circuit (Fig. 1, label 23, Abstract discloses "a comparison circuit 23 for inputting and comparing count values of the counters 21 and 22 and outputting a control signal in an active state when the count value of the counter 21 is a first value and the count value of the counter 22 is the first value.").

c. **Claim 25**, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator circuit asserts a lock signal when the voltage across the capacitor exceeds the reference signal (see part 3 and figure 2). The combined invention of Lee, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990 does not disclose expressly the capacitor charges slowly and discharges quickly, thus the rate of capacitor charge would be slower than the rate of discharge since the capacitor charges slowly and discharges quickly. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a capacitor which charges slowly and discharges quickly. Applicant has not disclosed that the capacitor charges slowly and discharges quickly provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would

have expected Applicant's invention to perform equally well with Hirai, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990. Therefore, it would have been obvious to one of ordinary skill in this art to modify Hirai, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990 to obtain the invention as specified in claim 25.

d. **Claim 26**, IBM Technical Disclosure Bulletin, May 1990 discloses comparator asserts a lock signal when the reference signal exceeds the voltage across the capacitor see part 3 and figure 2). The combined invention of Lee, Van Roon, and the IBM Technical.

Disclosure Bulletin, May 1990 does not disclose expressly the capacitor

charges slowly and discharges quickly, thus the rate of charging the capacitor would be faster than the rate of the discharge since the capacitor charges slowly and discharges quickly. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a capacitor which charges quickly and discharges slowly. Applicant has not disclosed that the capacitor charges quickly and discharges slowly provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with Hirai, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990. Therefore, it would have been obvious to one of ordinary skill in this art to modify Hirai, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990 to obtain the invention as specified in claim 25.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
    a. Meltzer (US Publication No.: 20030112915)
    b. Lee (US Publication No.: 20020094054)
    c. Eom (US Publication No.: 20020084859)
    d. Nishimura et al (US Patent No.: 6392641).
15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

16. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong
6/6/2008

/David C. Payne/

Supervisory Patent Examiner, Art Unit 2611